REMARKS

Claims 1-4, 6-20 and 22-37 are pending in this application. By this Amendment, claim 3 is amended to correct a previous change.

Entry of the amendment is proper under 37 C.F.R. §1.116 because the amendment: (1) places the application in condition for allowance; (2) does not raise any new issues requiring further search and/or consideration; and/or (3) places the application in better form for appeal, should an appeal be necessary. More specifically, the amendment merely corrects a previous amendment. No new issues are raised. Entry is thus proper under 37 C.F.R. §1.116.

The Office Action rejects claims 1-37 under 35 U.S.C. §103(a) by U.S. Patent 5,365,475 to Matsumura et al. (hereafter Matsumura) and U.S. Patent 4,567,577 to Oliver. The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites a first transistor pair coupled between a supply voltage line and GROUND, a second transistor pair coupled between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage based on a first mode of the memory device and to receive a second supply voltage based on a second mode of the memory device, the second supply voltage being different than the first supply voltage. Independent claim 1 also recites a first access transistor, a second access transistor and a bias transistor. The bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a non-ACTIVE mode/state.

The applied references do not teach or suggest at least these features of independent claim 1. The Office Action states that Matsumura does not teach or suggest the claimed bias transistor as recited in independent claim 1 (as well as the claimed switching device recited in other claims). The Office Action then relies on Oliver's n-channel transistor 35 (FIG. 2) as corresponding to the claimed bias transistor. However, Oliver's transistor 35 does not teach or suggest to apply a forward body bias to one of the n-channel transistors 25 or 27. Furthermore, Oliver's transistor 35 does not teach or suggest to apply forward body bias to one of the transistors 25 or 27 based on a non-ACTIVE mode/state.

Despite applicant's previous argument, the Office Action still does not specifically address the claimed features relating to a forward body bias (such as being applied by the alleged transistor 35 in Oliver's FIG. 2).

Forward body bias is a term that is well known to one skilled in the art (and is discussed in the present specification). For example, a forward body bias may occur to an n-channel transistor (such as Oliver's transistors 25 and 27) when a voltage applied to a body of the transistor is higher than a voltage at a source of the transistor. Additionally, with respect to an example in the present specification, a forward body bias may be applied to transistors 302 and 312 (FIG. 5) based on transistor 340 being turned ON (and thereby being coupled to GROUND) and based on sources of the transistors 302 and 312 being coupled to a voltage on VCC signal line 310 (which may vary based on a mode or state of the memory device).

Oliver's transistor 25 (and 27) includes a source coupled to VSS and a drain coupled to a transistor 24 (and ultimately to VDD). The transistor 35 (i.e., the alleged bias transistor) is turned on when the WRITE line 38 is inactive, and then the substrate of the transistor 25 is effectively coupled to VSS (through the transistor 35). Therefore, both the source and substrate of the transistor 25 are coupled to VSS. Accordingly, there is no suggestion to apply a forward body bias to the transistor 25 (and 27) when the WRITE line 38 is inactive.

Stated differently, a voltage VSS is applied to substrates of the transistors 25 and 27 and a voltage VSS is applied to sources of the transistors 25 and 27. Thus, a substantially same voltage (VSS) is applied to both the source and substrate of the transistors 25 and 27. This does not correspond to a bias transistor to apply a forward body bias (as would be known to one skilled in the art).

The Office Action (on page 3, line 2) also states that Oliver's transistor 35 applies a forward negative bias voltage VSS to the transistors 25 and 27. However, the terminology of a forward negative bias voltage is never used in Oliver. Applicant respectfully submits that there is no basis for the naming of the voltage VSS as "forward negative." Oliver does not apply a forward body bias based on WRITE line 38 being inactive.

Further, the Office Action appears to have incorrectly described Oliver's description. For example, the Office Action appears to state the applying of voltage VSS to the substrate of the transistors 25/27 is called a body effect and that Oliver uses a back gate bias to control the transistors. The terminology of the back gate bias and body effect is described at col. 3, lines 14-20. However, this terminology is discussed with respect to the transistor 36 being turned on (and the transistor 35 being off). See col. 3, lines 10-14.

Stated differently, the body effect is based on a WRITE line 38 being active (and not the WRITE line 38 being inactive). Thus, the Office Action's reference to body effect and/or back gate bias appears to be improper.

The Office Action further identifies the body effect during a non-active WRITE mode/state as motivation to combine Matsumura and Oliver. However, the alleged body effect occurs when the WRITE line 38 is active (and thus not when the WRITE signal being inactive). Thus, the Office Action's alleged motivation actually teaches away from the claimed features. The Office Action therefore does not provide proper motivation to combine Matsumura and Oliver.

There is no suggestion to combine Matsumura and Oliver as alleged in the Office Action. That is, Matsumura relates to different voltages (V1, V2) being applied to p-channel transistors 21 and 22. See Matsumura's FIG. 3. In contrast, Oliver applies constant voltages VSS and VDD as well as applies a voltage VSS to the substrate of the n-channel transistors 25 and 27. There is no suggestion of how to combine Oliver's voltage VSS being applied to substrate of the n-channel transistors with Matsumura's p-channel transistors that receive voltages V1/V2. These are different principles of operations (and there is no suggestion in the prior art to combine those principles). Additionally, there is no suggestion in the prior art to modify Matsumura so as to include providing a varying potential to substrates of transistors (such as is alleged within Oliver). The only suggestion for the claimed features is provided in applicants' own specification. The Office Action clearly relies on impermissible hindsight by relying on applicants' own specification in order

to combine Matsumura and Oliver. The Office Action therefore fails to make a *prima facie* case of obviousness.

For at least the reasons set forth above, the applied references do not teach or suggest all the features of independent claim 1. Thus, independent claim 1 defines patentable subject matter.

Independent claim 9 also defines patentable subject matter for at least similar reasons. That is, independent claim 9 recites a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell. For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features. Thus, independent claim 9 defines patentable subject matter.

Independent claim 18 also defines patentable subject matter for at least similar reasons as set forth above. That is, independent claim 18 recites a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a first voltage level in a first mode and to apply a second voltage level in a second mode, the SRAM device including a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of either the first mode or the second mode of the SRAM device. For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 18. Additionally, Oliver clearly does not suggest to apply a forward body bias based on a signal provided by a power control unit (that also applies a first voltage level in a first mode and

applies a second voltage level in a second mode). Also, there is no suggestion to combine Matsumura and Oliver so as to relate to the specifically claimed features of the power control unit. Accordingly, independent claim 18 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 9 and 18 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

For example, dependent claim 6 relates to a STANDBY signal. More specifically, dependent claim 6 recites a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of a STANDBY state of the memory device. The Office Action appears to state that the WRITE line being inactive is inherently present only during a non-ACTIVE WRITE mode/state. However, as stated in MPEP §2112, to establish inherency, the evidence must make clear that the missing matter is necessarily present in the thing described in the reference. The mere fact that a certain thing may result for a given set of circumstances is not sufficient. Oliver's WRITE line being inactive does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. This is, the present application clearly describes a STANDBY signal and a STANDBY state of a memory device. One skilled in the art would clearly know that Oliver's WRITE line signal, or lack of the WRITE line signal, does not necessarily correspond to a STANDBY signal indicative of a STANDBY state of a memory device. Rather, Oliver's WRITE line signal merely relates to whether data is being written. The lack of a WRITE line signal does

not necessarily correspond to a STANDBY state of a memory device. Therefore, the claimed features are not inherent. Despite applicants' previous arguments with respect to this issue, the Office Action still has not addressed this specific feature of dependent claim 6. Thus, dependent claim 6 defines patentable subject matter at least for this additional reason.

Each of dependent claims 7, 14, 15, 22-29 and 31-34 also relate to a STANDBY mode. Oliver does not teach or suggest these features for at least the reasons set forth above. Each of these dependent claims defines patentable subject matter at least for this additional reason.

Still further, dependent claim 4 recites the bias transistor applies the forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a mode of the memory device. Oliver does not teach or suggest that the transistor 35 applies a forward body bias based on a mode of the memory device. That is, a WRITE line being inactive is not a mode of a memory device. Dependent claim 4 defines patentable subject matter at least for this additional reason.

Additionally, dependent claim 12 recites the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to the power control unit. Oliver does not teach or suggest these features. More specifically, Oliver's transistor 35 does not include a gate coupled to a power control unit (where the power control unit to change the supply voltage on the supply voltage line based on either the first mode or the second mode and the power control unit further to control switching of the switching device based on either the first mode or the second mode of the first SRAM memory cell).

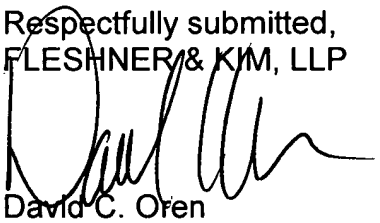
Dependent claim 12 defines patentable subject matter at least for this additional reason.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-4, 6-20 and 22-37 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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